IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	Examiner: Idriss N. Alrobaye
Paul L. Master, et al.	)	
	)	Group Art Unit: 2183
Appl. No.: 09/997,530	)	
	)	
Filed: November 30, 2001	)	
	)	
For: APPARATUS, SYSTEM AND METHOD FOR CONFIGURATION OF ADAPTIVE INTEGRATED CIRCUITRY HAVING FIXED, APPLICATION SPECIFIC COMPUTATIONAL ELEMENTS	)	

MS Appeals
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Commissioner:

This Appeal Brief is filed pursuant to the Appellants' appeal to the Board of Patent Appeals and Interferences ("Board") from the rejection of claims 182-305 in the September 25, 2009 Final Office Action. (Exhibit B). A Notice of Appeal was filed on December 22, 2009. The due date for this Appeal Brief is two months from the mailing date of the Notice of Appeal and this brief is being filed with a one-month extension of time.

I. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, QST Holdings, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in an appeal of this matter.

III. STATUS OF THE CLAIMS

Claims 182-305 stand rejected and their rejection is the subject of the appeal of this matter. Claims 1-181 were previously canceled.

IV. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Amendment and Response to Office Action mailed June 22, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 182-305 include, but are not limited to, methods and systems to provide configuration information to configure and reconfigure an adaptive integrated circuit as demonstrated in the embodiments shown in Figs. 1-10 of the specification. Claim 182 generally relates to a system 100 for adaptive configuration. *See* Abstract, ¶ 2, Figs. 1, 2 and 4-9, U.S. Publication No. 2003/0102889[1] (Exhibit A), Specification, p. 1, ll. 9-12. The system 100 includes a memory 10, 15, 20 or 61 adapted to store configuration information including a first configuration information and a second configuration information. (Ex. A, ¶¶ 27, 32-34 and 71, Figs. 1-2, Specification, p. 6, ll. 22-30, p. 9, l. 10 to p. 10, l. 14, p. 26, l. 30 to p. 27, l. 11). A first computational unit 200 such as computational unit 200A has a configurable basic architecture including a first plurality of heterogeneous computational elements 250 such as elements 250A-D and a first interconnection network 220 configurably coupling the first

[1] The Publication for the application at issue is being attached for convenience as Exhibit A. Applicant is also providing the corresponding specification page and line number in this and following sections.

plurality of heterogeneous computational elements together. (Ex. A, ¶¶ 46, 54, and 56, Figs. 4-6, Specification, p. 15, l. 26 to p. 16, l. 7, p. 20, ll. 19-31, p. 22, ll. 7-19, p. 28, ll. 8-15). The first interconnection network 210 and 220 configures interconnections between the first plurality of heterogeneous computational elements 250 in response to the first configuration information to perform a basic computational function. (Ex. A, ¶¶ 47, 49-50, 58, and 67, Specification, p. 16, ll. 9-25, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 21, ll. 14-29, p. 25, ll. 6-25). A second computational unit 200 such as computational unit 200B has a configurable complex processing architecture including a second plurality of heterogeneous computational elements 250 such as elements 250E-250H and a second interconnection network 220 configurably coupling the second plurality of heterogeneous computational elements 250 together. (Ex. A, ¶¶ 46, 54, and 56, Figs. 4-6, Specification, p. 15, l. 26 to p. 16, l. 7, p. 20, ll. 19-31, p. 21, ll. 14-29, p. 22, ll. 7-19). The second interconnection network configures interconnections between the second plurality of heterogeneous computational elements 250 in response to the second configuration information to perform a complex processing function. (Ex. A, ¶¶ 47, 49-50, 58, 67 and 75, Specification, p. 16, ll. 9-25, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 21, ll. 14-29, p. 25, ll. 6-25, p. 28, ll. 8-15).

Claim 213 generally relates to a system 100 for adaptive configuration. (Ex. A, Abstract, ¶ 2, Figs. 1, 2 and 4-9, Specification, p. 1, ll. 9-12). The system includes a memory 10, 15, 20 or 61 adapted to store configuration information including a first configuration information and a second configuration information. (Ex. A, ¶¶ 27, 32, 34 and 71, Figs. 1-2, Specification, p. 6, ll. 22-30, p. 9, l. 10 to p. 10, l. 14, p. 26, l. 30 to p. 27, l. 11). A first configurable basic computational logic unit 200 such as unit 200A includes a first plurality of heterogeneous computational elements 250 such as elements 250A-D and a first interconnection network 220

for forming a first configurable architecture. (Ex. A, ¶¶ 46, 54 and 56, Figs. 4-6, Specification, p. 15, l. 26 to p. 16, l. 7, p. 20, ll. 19-31, p. 22, ll. 7-19, p. 28, ll. 8-15). The first interconnection network 220 configurably couples the first plurality of heterogeneous computational elements 250 together and configures interconnections between the first plurality of heterogeneous computational elements 250 in response to the first configuration information to perform a basic computational function. (Ex. A, ¶¶ 47, 49-50, 58 and 67, Specification, p. 16, ll. 9-25, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 21, ll. 14-29, p. 25, ll. 6-25). A second configurable complex processing unit 200 such as unit 200B includes a second plurality of heterogeneous computational elements 250 such as elements 250E-250H and a second interconnection network 220 for forming a second configurable architecture. (Ex. A, ¶¶ 46, 54 and 56, Figs. 4-6, Specification, p. 15, l. 26 to p. 16, l. 7, p. 20, ll. 19-31, p. 22, ll. 7-19). The second interconnection network 220 configurably couples the second plurality of heterogeneous computational elements 250 together and configures interconnections between the second plurality of heterogeneous computational elements 250 in response to the second configuration information to perform a complex processing function. (Ex. A, ¶¶ 47, 49-50, 58, 67 and 75, Specification, p. 16, ll. 9-25, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 21, ll. 14-29, p. 25, ll. 6-25, p. 28, ll. 8-15).

Claim 246 generally relates to a method for adaptive configuration of an integrated circuit 100. (Ex. A, Abstract, ¶ 2, Fig. 10, Specification, p. 1, ll. 9-12). Configuration information is received. (Ex. A, ¶ 88, element 830 Fig. 10, Specification, p. 32, l. 30 to p. 33, l. 5). The configuration information is stored in a memory 10, 15, 20 or 61. (Ex. A, ¶¶ 27, 32, 34 and 71, Figs. 1-2, Specification, p. 6, ll. 22-30, p. 9, l. 10 to p. 10, l. 14, p. 26, l. 30 to p. 27, l. 11). In response to the configuration information, interconnections are configured between a

first plurality of heterogeneous computational elements 250 of the integrated circuit 100 via a first interconnection network 220 of the integrated circuit 100 to provide a configurable basic computational unit 200 such as unit 200A to perform a basic computational function. (Ex. A, ¶¶ 46-47, 49-50, 52, 54, 56 and 58, Figs. 4-6, Specification, p. 15, l. 18 to p. 16, l. 16, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 19, ll. 10-19, p. 20, ll. 19-31, p. 21, ll. 14-29). The first interconnection network 220 configurably couples the first plurality of heterogeneous computational elements together 250. (Ex. A, ¶¶ 47, 54 and 67, Fig. 4, Specification, p. 16, ll. 8-16, p. 20, ll. 19-31, p. 25, ll. 6-12). Interconnections are configured between the second plurality of heterogeneous computational elements 250 of the integrated circuit via the second interconnection network 220 of the integrated circuit to provide a configurable complex computational unit such as the unit 200B to perform a complex processing function. (Ex. A, ¶¶ 46-47, 49-50, 52, 54, 56, 58 and 75, Figs. 4-6, Specification, p. 15, l. 18 to p. 16, l. 16, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 19, ll. 10-19, p. 20, ll. 19-31, p. 21, ll. 14-29, p. 28, ll. 8-15). The second interconnection network 220 configurably couples the second plurality of heterogeneous computational elements 250 together. (Ex. A, ¶¶ 47, 54 and 67, Fig. 4, Specification, p. 16, ll. 8-16, p. 20, ll. 19-31, p. 25, ll. 6-12).

Claim 276 generally relates to a method for adaptive configuration of an integrated circuit 100. (Ex. A, Abstract, ¶ 2, Fig. 10, Specification, p. 1, ll. 9-12). The integrated circuit 100 has a first plurality of heterogeneous computational elements 250 such as elements 250A-D, a second plurality of heterogeneous computational elements 250 such as elements 250E-H, and an interconnection network 220 coupled to memory 10, 15, 20 or 61. (Ex. A, ¶¶ 27, 34, 46, 54, 56 and 71 Figs. 4-6, Specification, p. 6, ll. 22-30, p. 15, l. 26 to p. 16, l. 7, p. 20, ll. 19-31, p. 22, ll. 7-19, p. 28, ll. 8-15). An interconnection network configurably couples the first plurality of

heterogeneous computation elements 250 and a second interconnection network configurably couples the second plurality of heterogeneous computational elements together. (Ex. A, ¶¶ 47, 49-50, 58, 67 and 75, Specification, p. 16, ll. 9-25, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 21, ll. 14-29, p. 25, ll. 6-25, p. 28, ll. 8-15). Configuration information is transmitted and received by the elements. (Ex. A, ¶¶ 71, 88, element 830 Fig. 10, Specification, p. 26, l. 23 to p. 27, l. 3, p. 32, l. 30 to p. 33, l. 5). The received configuration information is stored in a memory 10, 15, 20 or 61. (Ex. A, ¶¶ 27, 32, 34 and 71, Figs. 1-2, Specification, p. 6, ll. 22-30, p. 9, l. 10 to p. 10, l. 14, p. 26, l. 30 to p. 27, l. 11). In response to the configuration information, interconnections are configured between a first plurality of heterogeneous computational elements 250 via a first interconnection network 220 to provide a configurable basic computational unit 200 to perform a basic computational function. (Ex. A, ¶¶ 46-47, 49-50, 52, 54, 56 and 58, Figs. 4-6, Specification, p. 15, l. 18 to p. 16, l. 16, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 19, ll. 10-19, p. 20, ll. 19-31, p. 21, ll. 14-29). The first interconnection network 200 configurably couples the first plurality of heterogeneous computational elements together. (Ex. A, ¶¶ 47, 54 and 67, Fig. 4, Specification, p. 16, ll. 8-16, p. 20, ll. 19-31, p. 25, ll. 6-12). Interconnections are configured between a second plurality of heterogeneous computational elements 250 via a second interconnection network 220 to provide a configurable complex computational unit to perform a complex processing function. (Ex. A, ¶¶ 46-47, 49-50, 52, 54, 56, 58 and 75, Figs. 4-6, Specification, p. 15, l. 18 to p. 16, l. 16, p. 17, ll. 3-22, p. 17, l. 30 to p. 18, l. 2, p. 19, ll. 10-19, p. 20, ll. 19-31, p. 21, ll. 14-29, p. 28, ll. 8-15). The second interconnection network configurably couples the second plurality of heterogeneous computational elements together. (Ex. A, ¶¶ 47, 54 and 67, Fig. 4, Specification, p. 16, ll. 8-16, p. 20, ll. 19-31, p. 25, ll. 6-12).

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

I. Whether claims 182-246, 248-276 and 278-305 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,768,561 ("Wise" attached as Exhibit C) in view of U.S. Patent No. 5,794,062 ("Baxter" attached as Exhibit D).

II. Whether claims 247 and 277 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Wise and Baxter in view of the U.S. Patent No. 6,005,943 ("Cohen" attached as Exhibit E).

With regard to claims 182, 213, 246 and 276 the Final Office Action asserts that Wise teaches a system for adaptive configuration. (Ex. B, p. 2). The Final Office Action cites Fig. 137 of Wise as disclosing "a first computation unit having a first plurality of heterogeneous computation elements in the form of a carry-save multiplier, a carry save adder and a carry save subtractor." (Ex. B, p. 3). The Final Office Action asserts that Wise discloses a first interconnection network configuring interconnections between the heterogeneous computational elements citing Fig. 137 and Col. 262, ll. 14-42. (Ex. B, p. 3). The Final Office Action notes that Wise discloses a second computation unit with a configurable complex processing architecture citing Col. 6, ll. 57-67 and Col. 7, ll. 1-12. (Ex. B, p. 3). The Final Office Action notes that Wise discloses a second interconnection network configuring interconnections between the computational elements citing Col. 262, ll. 14-42 in relation to Fig. 137. (Ex. B, p. 3). The Final Office Action concedes that Wise does not disclose a memory adapted to store first and second configuration information. (Ex. B, p. 4). The Final Office notes that Baxter teaches a memory for storing first and second configuration. (Ex. B, p. 4).

VII. ARGUMENT

For the Board's convenience, claims 182-305 are one group that will stand or fall together. As will be explained, the Final Office Action fails to meet the burden to establish that the combination of Wise and Baxter disclose all of the elements of the independent claims 183, 213, 246 and 276 and their corresponding dependent claims.

A Claims 182-246, 248 and 278-305 Were Improperly Rejected Under 35 U.S.C. 103(a) As Unpatentable Over Wise In View Of Baxter

1. The Concepts Of Hardware Reconfigurability, Heterogeneous Computational Elements And An Interconnection Network

The claims at issue in this appeal all relate to the configuration of hardware computational elements via the switching of connections between such elements via an interconnection network according to configuration information. This captures the flexibility of software to perform multiple programmed tasks and the speed of pure hardware that is dedicated to specific functions. As explained by the specification:

> The related application discloses a new form or type of integrated circuitry which effectively and efficiently combines and maximizes the various advantages of processors, application specific integrated circuits ("ASICs"), and field programmable gate arrays ("FPGAs"), while minimizing potential disadvantages. The related application illustrates a new form or type of integrated circuit ("IC"), referred to as an adaptive computing engine ("ACE"), which provides the programming flexibility of a processor, the post-fabrication flexibility of FPGAs, and the high speed and high utilization factors of an ASIC. This ACE integrated circuitry is readily reconfigurable, is capable of having corresponding, multiple modes of operation, and further minimizes power consumption while increasing performance, with particular suitability for low power applications, such as for use in hand-held and other battery-powered devices.

(Ex. A, ¶ 3, Spec. p. 1, l. 3 to p. 2, l. 2, emphasis added). A critical aspect of the claims is the interconnection network that allows for the configuration of computational elements of a computational unit by changing connections between the computational elements to have the computational unit perform different functions. The specification details this feature as distinct from prior art connections such as bus types:

> In the preferred embodiment, the various interconnection networks are implemented as described, for example, in U.S. Pat. No. 5,218,240, U.S. Pat. No. 5,336,950, U.S. Pat. No. 5,245,227, and U.S. Pat. No. 5,144,166, and also as discussed below and as illustrated with reference to FIGS. 7, 8 and 9. These various interconnection networks provide selectable (or switchable) connections between and among the controller 120, the memory 140, the various matrices 150, and the computational units 200 and computational elements 250 discussed below, providing the physical basis for the configuration and reconfiguration referred to herein, in response to and under the control of configuration signaling generally referred to herein as "configuration information". In addition, the various interconnection networks (110, 210, 240 and 220) provide selectable, routable or switchable data, input, output, control and configuration paths, between and among the controller 120, the memory 140, the various matrices 150, and the computational units 200 and computational elements 250, in lieu of any form of traditional or separate input/output busses, data busses, DMA, RAM, configuration and instruction busses.

(Ex. A, ¶ 41, Spec. p. 13, ll. 7-20, emphasis added). Another distinct feature is the use of different or heterogeneous computational elements such as adders, multipliers, functional generators, filters, etc. that allow multiple functions to be performed efficiently without a one size fit all homogeneous element that limit the flexibility of a traditional FPGA. As explained by the specification:

> The next and perhaps most significant concept of the present invention, and a marked departure from the concepts and precepts of the prior art, is the concept of reconfigurable "heterogeneity" utilized to implement the various selected algorithms mentioned above. As indicated in the related application, prior art reconfigurability has relied exclusively on homogeneous FPGAs, in which identical blocks of logic gates are repeated as an array within a rich, programmable interconnect, with the interconnect subsequently configured to provide connections between and among the identical gates to implement a particular function, albeit inefficiently and often with routing and combinatorial problems. In stark contrast, in accordance with the present invention, within computation units 200, different computational elements (250) are implemented directly as correspondingly different fixed (or dedicated) application specific hardware, such as dedicated multipliers, complex multipliers, and adders. Utilizing interconnect (210 and 220), these differing, heterogeneous computational elements (250) may then be adaptively configured, in advance, in real-time or at a slower rate, to perform the selected algorithm, such as the performance of discrete cosine transformations often utilized in mobile communications. As a consequence, in accordance with the present invention, different ("heterogeneous") computational elements (250) are configured and reconfigured, at any given time, to optimally perform a given algorithm or other function. In addition, for repetitive functions, a given instantiation or configuration of computational elements may also

> remain in place over time, i.e., unchanged, throughout the course of such repetitive calculations.

(Ex. A, ¶ 46, Spec. p. 15, l. 18 to p. 16, l. 7, emphasis added). The use of configuration information in conjunction with these features provides the advantage of use of the hardware even for newer standards that would require either brand new integrated circuits if using ASICs or extensive rewiring if using a traditional FPGA. As the specification explains:

> The temporal nature of the ACE 100 architecture should also be noted. At any given instant of time, utilizing different levels of interconnect (110, 210, 240 and 220), a particular configuration may exist within the ACE 100 which has been optimized to perform a given function or implement a particular algorithm, such as to implement pilot signal searching for a CDMA operating mode in a mobile station 30 or 32. At another instant in time, the configuration may be changed, to interconnect other computational elements (250) or connect the same computational elements 250 differently, for the performance of another function or algorithm, such as multipath reception for a CDMA operating mode. Two important features arise from this temporal reconfigurability. First, as algorithms may change over time to, for example, implement a new technology standard, the ACE 100 may co-evolve and be reconfigured to implement the new algorithm. Second, because computational elements are interconnected at one instant in time, as an instantiation of a given algorithm, and then reconfigured at another instant in time for performance of another, different algorithm, gate (or transistor) utilization is maximized, providing significantly better performance than the most efficient ASICs relative to their activity factors. This temporal reconfigurability also illustrates the memory functionality inherent in the MIN 110, as mentioned above.

(Ex. A, ¶ 47, Spec. p. 16, ll. 8-25, emphasis added).

Another advantage is the diversity of computational units since they are made of different types of computational elements and can be specialized for performing different types of functions. For example, the claims require a first type of computational unit that performs basic computational functions and a complex processing computational unit having computational elements that are designed for more complex operations such as higher order mathematical calculations or digital signal processing functions. Such configurable units have advantages over an FPGA configured for more complex functions because they eliminate unnecessary interconnection hardware as well as performance inefficiencies from having only one type of

computational unit. Further since all of the computational units are configurable, they may be adapted to new standards by simply changing the connections between the computational elements.

For example, Fig. 4 shows different computational elements 250A-N making up different types of computational units 200. Certain of the computational units 200 perform simple processing (e.g. such as "bit level manipulation" as explained in p. 21, ll. 14-39 of the specification, Ex. A, ¶ 56) and certain of the computational elements 200 perform word level processing (e.g. multiplication, cosine transformation, etc.) that operate at a more complex level (multiple bits). A more detailed example of a configured simple computational unit is shown in Fig. 8. A more detailed example of different configurations of a complex computational unit is shown in Figs. 6A-6D. The interconnection networks 210 and 220 in Figs. 3-4 allows any of the combination of computational elements 250 in the computational units 200 shown in these figures to be connected to form the combinations in the claims as explained in p. 11, ll. 10-15 of the specification. (Ex. A, ¶ 41).

The claimed subject matter therefore offers unique features that are not present in circuits such as Wise that may have multiple functions but cannot be "configured" for new standards.

2. Wise and Baxter Represent Prior Art Systems That Do Not Include Critical Elements of The Independent Claims

The main cited references, Wise and Baxter, are both prior art systems of types that the specification discusses and dismisses. Wise is generally directed toward a hardware implemented video decompression circuit. (Ex. C, Abstract). Although Wise makes reference to "reconfiguration," such reconfiguration is not performed using an interconnection network to change interconnections between different computational elements as required by the present

claims. Instead the reconfiguration references specific functions that are achieved in the integrated circuit and selected via instructions from tokens. However, new instructions that are not part of the instruction set could not reconfigure the connections between the elements in the circuit on Wise to perform new functions. Wise is more of the nature of an ASIC that has limited functions and cannot be reconfigured to perform new, unplanned functions.

The Final Office Action has cited the inverse discrete cosine transform (IDCT) block shown in Fig. 137 of Wise as disclosing a first computational units having computational elements such as the carry-save multiplier, carry save adder and carry save subtractor. (Ex. B, p. 3). The Final Office Action has characterized Fig. 137 as disclosing a first interconnection network that configures interconnections between the blocks citing Col. 262, ll. 14-42 of Wise. (Ex. B, p. 3). This section is actually is a summary of various components in Fig. 137 but does not disclose an interconnection network allowing changing connections between the different components in Fig. 137.

Wise contains a lengthy specification that is broken up into various sections. Cols. 42-77 describe different functions of the overall system. Section A explains various functions that may be performed that are associated with tokens that communicate information to the decoder chip set. (Ex. C, Cols. 78-195). Section B describes the hardware for the start code detector which performs specific discrete functions. (Ex. C, Col. 195, ll. 16-26). Fig. 137 of Wise is a part of the start code detector and actually shows the inverse discrete cosine transform (IDCT) block of the code detector. (Ex. C, Col. 259, ll. 35-51). The IDCT block is the equivalent of an ASIC as it is designed to perform the function of an inverse discrete cosine transform that cannot be reconfigured to perform any other functions. The overall architecture in Fig. 137 makes it clear that there is no interconnection network since none of the connections shown between the

various adders, subtractors and multipliers may be changed. The IDCT block in Fig. 137 may perform only a single function related to the cosine transform and cannot be configured. Finally, Fig. 137 does not describe two computational units, it is at best a single computational unit that performs a singular function.

Baxter generally relates to a repeated array of S-machines and T-machines that are connected by a matrix with corresponding input devices. (Ex. D, Col. 4, ll. 55-65). Baxter is typical of known FPGA art that required massive interconnection infrastructure in the FPGAs that make up the dynamically reconfigurable processing unit (DRPU) 32 of the S-Machine 12 and the FPGA that makes up the T-Machines 18. (Ex. D, Col. 5, ll. 14-16, Col. 6, ll. 8-19, Col. 10, ll. 46-59). The Final Office Action has cited Fig. 3A and 4 of Baxter as disclosing a memory for storing first and second configuration information. (Ex. B, p. 4). As noted above, the memory 34 of a given S-machine includes complex configuration instructions necessary for an FPGA which makes up the DRPU 32. (Ex. D, Col. 11, ll. 38-47). Baxter makes clear that the configuration is used for an FPGA which is composed of homogeneous (identical) computational elements and therefore is significantly different from the present claims. (Ex. D, Col. 15, ll. 34-66).

3. Claims 183, 213, 246 and 276 Are Allowable Because Wise Does Not Disclose A First Computational Unit And A Second Computational Unit

Claims 183, 213, 246 and 276 require a first computational unit having a configurable basic architecture and a second computational unit having a configurable complex processing architecture. The Final Office Action has cited Fig. 137 of Wise as disclosing for both of these units. (Ex. B, p. 3). The block shown in Fig. 137 is a single computational unit and cannot be separated into two computational units each performing separate functions and therefore does not

anticipate these claim elements. The Final Office Action has cited Col 6, ll. 57-67 and Col. 7, ll. 1-12 of Wise for complex multiplication and the x [2,5] output of Fig. 137 as showing a second functional mode. (Ex. B, p. 3). Applicant respectfully submits that this is an incorrect reading of Wise. Col. 6, l. 57 to Col. 7, l. 12 generally describes the different functions along various processing stages but does not disclose how the processing stages are configured via the tokens. (Ex. C). As explained above, the "configuration" refers to predetermined alternate functions which do not use configuration information to change the interconnections between the computational elements such as multipliers and adders in Fig. 137.

The output designated by x [2,5] in Fig. 137 does not disclose configuration based on changing interconnections. Examining Fig. 137 shows that the output x [2,5] is simply one of four outputs that uses all of the components in the architecture in a pre-designated fashion to transform 4 separate matrix outputs. As explained by Col. 261, ll. 2-40, the circuit components in Fig. 137 are mapped to perform a specific one-dimensional algorithm that is performed multiple times to achieve a two-dimensional discrete cosine transform. (Ex. C). Fig. 136 shows the circuit for the one-dimensional transform of eight various Y values which are each transformed into corresponding x values. (Ex. C). The architecture in Fig. 137 is two-dimensional insofar as it is essentially used twice in order to obtain two sets of values thus saving various components in Fig. 136 that would be necessary to perform all eight transformations. There is no difference in the functions that produce a single output of the four outputs twice in Fig. 137. Therefore Wise does not disclose a second discrete computational unit since the architecture in Fig. 137 is simply reused for a second round of four inputs rather than a circuit that performs all eight transforms simultaneously as in Fig. 136. Wise does not disclose a first and second computational unit and therefore does not anticipate the claims.

The lack of disclosure of two discrete computational units may best be illustrated by comparing Fig. 136 to Fig. 137. Fig. 136 is a circuit that performs the transform of the eight x values into eight y-values as shown below. For example y [0] is transformed into x [0], y [4] is transformed into x [1], y [6] is transformed into x [2]. In contrast, these functions are also performed by the circuit in Fig. 137 which takes four y-values at a time and transforms them, thus resulting a reduction in the necessary circuitry because the circuitry in Fig. 137 is used twice and therefore produces the same eight x-values.

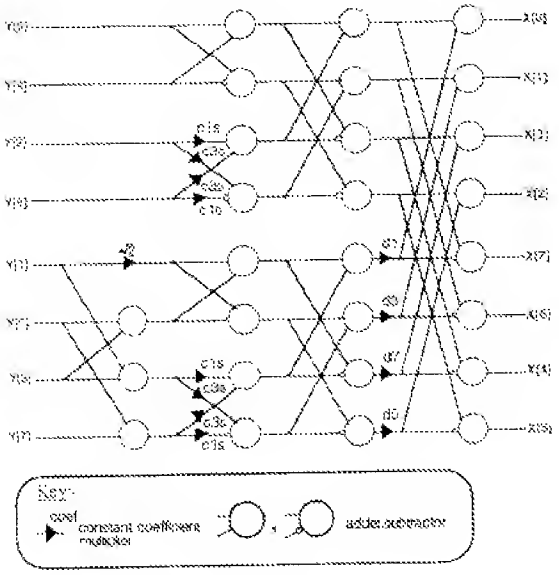

FIG. 136

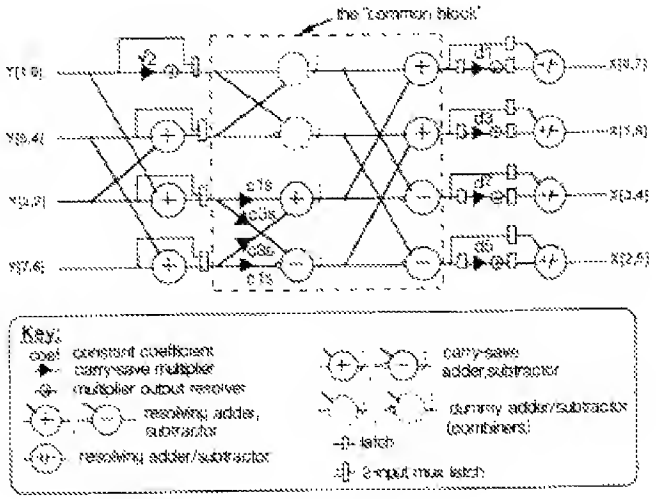

FIG. 137

The Office Action therefore is misconstruing operation of the circuit in Fig. 137. The IDCT in Fig. 137 is not two separate computational units since the entirety of the circuit performs a four value transformation twice. (Ex. C). Further, it is not "reconfigured" to perform a second function, the same function is simply performed twice ("reused") with different values to achieve the desired result of eight total cosine transformations. (Ex. C, Col. 262, l. 29). Since Fig. 137 and the remainder of Wise does not disclose two reconfigurable computational units, the claims are not anticipated by Wise or the combination of Wise with Baxter.

4. Claims 183, 213, 246 and 276 Are Allowable Because Wise Does Not Disclose An Interconnection Network

All of the independent claims require interconnection networks for each computational unit that each "configurably couple the respective plurality of computational elements" and for "configuring interconnections between" the computational elements in response to the configuration information. The Final Office Action has cited Fig. 137 of Wise as disclosing such an interconnection network. However, the Final Office Action has not provided any explanation of what elements in Fig. 137 constitute an interconnection network, let alone a network that may configure the interconnections between the computational elements. An examination of Fig. 137 shows that the connections between the various adders, multipliers and subtractors are permanent wired connections and therefore the connections cannot be changed. Further the connections are more akin to a bus rather than a true network that may route data between each computational elements. Even if certain routing may be performed via latches, the set of connections is fixed and data may only be routed to certain computational elements. The configuration in Fig. 137 therefore is not a network because it cannot configure the interconnections between the computational elements. Since Wise does not disclose an interconnection network, let alone one which changes the interconnections between the computational elements, Wise does not anticipate the pending claims.

B. Claims 247 and 277 Were Improperly Rejected Under 35 U.S.C. 103(a) As Unpatentable Over Wise and Baxter In View Of Cohen

Claims 247 and 277 are allowable over Wise, Baxter and Cohen for the same reasons that base independent claims 246 and 276 are allowable as explained in the section above.

VIII. CLAIMS APPENDIX

A clean copy of the claims 183-305 involved in the appeal is included in the Claims Appendix.

IX. EVIDENCE APPENDIX

A copy of the evidence relied upon by the appellant is included in the Evidence Appendix and is herein referenced. A list of evidence and where each was entered in the record is included in the Index to the Appendices.

X. RELATED PROCEEDINGS APPENDIX

As there are no related proceedings, no information is provided in the Related Proceedings Appendix.

XI. CONCLUSION

For at least the foregoing reasons, the final rejection of appealed claims 183-305 set forth in the Final Office Action mailed September 25, 2009, should be reversed.

Respectfully submitted,

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CLAIM APPENDIX

CLAIM APPENDIX
CLEAN COPY OF CLAIMS ON APPEAL

182. A system for adaptive configuration, the system comprising:

a memory adapted to store configuration information including a first configuration information and a second configuration information;

a first computational unit having a configurable basic architecture including a first plurality of heterogeneous computational elements and a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together, the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second computational unit having a configurable complex processing architecture including a second plurality of heterogeneous computational elements and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

183. The system of claim 182, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

184. The system of claim 182, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

185. The system of claim 182, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

186. The system of claim 182, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

187. The system of claim 182, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

188. The system of claim 182, wherein the system is embodied within an integrated circuit.

189. The system of claim 182, wherein the computational units are organized in a configurable computing matrix and the computing matrix is coupled to a matrix interconnection network.

190. The system of claim 189, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

191. The system of claim 189, wherein a first configured function of the configurable computing matrix is as a controller.

192. The system of claim 190, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

193. The system of claim 191, wherein the controller is a RISC controller.

194. The system of claim 182, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

195. The system of claim 194, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

196. The system of claim 182, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

197. The system of claim 182, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

198. The system of claim 182, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

199. The system of claim 198, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

200. The system of claim 199, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

201. The system of claim 197, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

202. The system of claim 196, wherein the first computational unit operates at a bit level; and

wherein the second computational unit operates at a word level.

203. The system of claim 202, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

204. The system of claim 182, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

205. The system of claim 204, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

206. The system of claim 205, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

207. The system of claim 206, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

208. The system of claim 207, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

209. The system of claim 182, further comprising a third interconnection network coupled to the first computational unit and the second computational unit, the third interconnection network sending the configuration information to the computational units.

210. The system of claim 209, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

211. The system of claim 182, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

212. The system of claim 211, wherein the configuration information includes control signals to control the multiplexers.

213. A system for adaptive configuration, the system comprising:

a memory adapted to store configuration information including a first configuration information and a second configuration information;

a first configurable basic computational logic unit including a first plurality of heterogeneous computational elements and a first interconnection network for forming a first configurable architecture, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second configurable complex processing unit including a second plurality of heterogeneous computational elements and a second interconnection network for forming a second configurable architecture, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together; the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

214. The system of claim 213, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

215. The system of claim 213, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

216. The system of claim 213, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

217. The system of claim 213, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

218. The system of claim 213, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

219. The system of claim 213, wherein the system is embodied within an integrated circuit.

220. The system of claim 213, wherein the logic unit and processing unit are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

221. The system of claim 220, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of logic and processing units.

222. The system of claim 213, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

223. The system of claim 220, wherein a first configured function of the configurable computing matrix is as a controller.

224. The system of claim 221, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

225. The system of claim 223, wherein the controller is a RISC controller.

226. The system of claim 213, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

227. The system of claim 226, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

228. The system of claim 213, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

229. The system of claim 213, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

230. The system of claim 213, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

231. The system of claim 230, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

232. The system of claim 231, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

233. The system of claim 229, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

234. The system of claim 228, wherein the first configurable basic computational logic unit operates at a bit level; and

wherein the second configurable complex processing unit operates at a word level.

235. The system of claim 234, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

236. The system of claim 213, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

237. The system of claim 236, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

238. The system of claim 237, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

239. The system of claim 238, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

240. The system of claim 239, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

241. The system of claim 213, further comprising a third interconnection network coupled to the first configurable basic computational unit and the second configurable complex processing unit, the third interconnection network sending the configuration information to the units.

242. The system of claim 241, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

243. The system of claim 213, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

244. The system of claim 243, wherein the configuration information includes control signals to control the multiplexers.

245. The system of claim 213, wherein the first interconnection network provides a third configuration information to reconfigure the first configurable basic computational unit to

perform a second computational function, the memory being adapted to store the third configuration information.

246. A method for adaptive configuration of an integrated circuit, the method comprising:

receiving configuration information;

storing the configuration information in a memory; and

in response to the configuration information:

configuring interconnections between a first plurality of heterogeneous computational elements of the integrated circuit via a first interconnection network of the integrated circuit to provide a configurable basic computational unit to perform a basic computational function, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; and

configuring interconnections between the second plurality of heterogeneous computational elements of the integrated circuit via the second interconnection network of the integrated circuit to provide a configurable complex computational unit to perform a complex processing function, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together.

247. The method of claim 246, further comprising requesting authorization to receive the configuration information.

248. The method of claim 246, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

249. The method of claim 246, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

250. The method of claim 246, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

251. The method of claim 250, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

252. The method of claim 246, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

253. The method of claim 250, wherein a first configured function of the configurable computing matrix is as a controller.

254. The method of claim 251, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

255. The method of claim 253, wherein the controller is a RISC controller.

256. The method of claim 246, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

257. The method of claim 250, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

258. The method of claim 246, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

259. The method of claim 246, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

260. The method of claim 246, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

261. The method of claim 260, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

262. The method of claim 261, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

263. The method of claim 259, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

264. The method of claim 258, wherein the configurable basic computational logic unit operates at a bit level; and

wherein the configurable complex processing unit operates at a word level.

265. The method of claim 264, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

266. The method of claim 246, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

267. The method of claim 266, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

268. The method of claim 267, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

269. The method of claim 268, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

270. The method of claim 269, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

271. The method of claim 246, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

272. The method of claim 271, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

273. The method of claim 246, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

274. The method of claim 273, wherein the configuration information includes control signals to control the multiplexers.

275. The method of claim 246, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

276. A method for adaptive configuration of an integrated circuit, the integrated circuit having a first plurality of heterogeneous computational elements, a second plurality of heterogeneous computational elements, and an interconnection network coupled to the memory, the interconnection network having and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the method comprising:

transmitting configuration information;

wherein the configuration information is received;

storing the received configuration information in a memory; and

in response to the configuration information:

configuring interconnections between a first plurality of heterogeneous computational elements via a first interconnection network to provide a configurable basic computational unit to perform a basic computational function, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; and

configuring interconnections between a second plurality of heterogeneous computational elements via a second interconnection network to provide a configurable complex computational unit to perform a complex processing function, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together.

277. The method of claim 276, further comprising requesting authorization to receive the configuration information.

278. The method of claim 276, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

279. The method of claim 276, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

280. The method of claim 276, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

281. The method of claim 280, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

282. The method of claim 276, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

283. The method of claim 280, wherein a first configured function of the configurable computing matrix is as a controller.

284. The method of claim 281, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

285. The method of claim 283, wherein the controller is a RISC controller.

286. The method of claim 276, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

287. The method of claim 286, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

288. The method of claim 276, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

289. The method of claim 276, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

290. The method of claim 276, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

291. The method of claim 290, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

292. The method of claim 291, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

293. The method of claim 289, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

294. The method of claim 288, wherein the configurable basic computational logic unit operates at a bit level; and

wherein the configurable complex processing unit operates at a word level.

295. The method of claim 294, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

296. The method of claim 276, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

297. The method of claim 296, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

298. The method of claim 297, wherein the basic computational function comprises it level manipulation; and

wherein the complex processing function comprises word level manipulation.

299. The method of claim 297, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

300. The method of claim 299, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

301. The method of claim 276, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

302. The method of claim 301, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

303. The method of claim 276, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

304. The method of claim 303, wherein the configuration information includes control signals to control the multiplexers.

305. The method of claim 276, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.